CLAIM LISTING

1. (Currently Amended) A method for storing macroblocks in a memory, said method comprising:

decoding a macroblock, thereby resulting in a decoded macroblock, said decoded macroblock comprising pixels; and

executing an instruction, wherein the instruction causes:

writing the decoded macroblock to the memory, wherein writing the macroblock to the memory further comprises:

writing a matrix of decoded luminance pixels to a first portion of the memory;

writing a first matrix of decoded chrominance pixels to a second portion of the memory;

writing a second matrix of decoded chrominance pixels to a third portion of the memory; and

the first portion, second portion, and third portion being contiguous; and

outputting a frame comprising said decoded macroblock to a display device.

2. (Cancelled)

3. (Currently Amended) A method for storing macroblocks in a memory, said method comprising:

decoding five macroblocks, thereby resulting in decoded macroblocks, said decoded macroblocks comprising pixels; and

executing an instruction, wherein the instruction causes:

writing the five macroblocks to the memory, wherein writing the macroblock to the memory further comprises:

writing five matrices of decoded luminance pixels to ~~a first portion of~~ the memory;

writing a first five matrices of decoded chrominance pixels to ~~a second portion of~~ the memory;

writing a second five matrices of decoded chrominance pixels to ~~a third portion of~~ the memory; and

the ~~first portion, second portion, and third portion~~ five matrices of decoded luminance pixels, the first five matrices of decoded chrominance pixels and the second five matrices of decoded chrominance pixels being stored contiguously in the memory ; and

outputting a frame comprising said five decoded macroblocks to a display device.

4. (Cancelled).

5. (Peviously Presented) A circuit for storing macroblocks, said circuit comprising:

a decoder for decoding macroblocks; and

a computer readable medium storing an executable instruction, wherein the instruction causes:

writing the macroblock to the memory, wherein writing the macroblock to the memory further comprises:

writing a matrix of decoded luminance pixels to a first portion of the memory;

writing a first matrix of decoded chrominance pixels to second portion of the memory;

writing a second matrix of decoded chrominance pixels to a third portion of the memory; and

the first portion, second portion, and third portion being contiguous.

6. (Cancelled).

7. (Previously Presented) A circuit for storing macroblocks, said circuit comprising:

a decoder for decoding five macroblocks, thereby resulting in decoded macroblocks, said decoded macroblocks comprising pixels; and

a computer readable medium storing an executable instruction, wherein the instruction causes:

writing the five macroblocks to the memory, wherein writing the macroblock to the memory further comprises:

writing five matrices of decoded luminance pixels to a first portion of the memory;

writing a first five matrices of decoded chrominance pixels to a second portion of the memory;

writing a second five matrices of decoded chrominance pixels to a third portion of the memory; and

the first portion, second portion, and third portion being contiguous.

8. (Cancelled).

9. (Currently Amended) The method of claim 1, wherein one portion of a single data word is part of the second portion of the memory where the first matrix of chroiminance pixels are written and another portion of the single data word is part of the third portion of the memory where the second matrix of chrominance pixels are written. ~~Form~~

10. (New) The method of claim 1, wherein the frame comprises a plurality of sequential macroblocks, and wherein periodic ones of the sequential macroblocks are stored at memory addresses that are offset by a power of 2.

11. (New) The method of claim 3, further comprising:

decoding another five macroblocks, thereby resulting in decoded another macroblocks, said decoded another macroblocks comprising pixels; and

executing an instruction, wherein the instruction causes:

writing the another five macroblocks to the memory, wherein writing the another five macroblocks to the memory further comprises:

writing another five matrices of decoded luminance pixels to the memory;

writing a another first five matrices of decoded chrominance pixels to the memory;

writing a another second five matrices of decoded chrominance pixels to the memory; and

wherein the another five matrices of decoded luminance pixels, another first five matrices of decoded chrominance pixels to the memory, and the another second five matrics of decoded chrominance pixels are written contiguously to the memory; and

wherein each one of the first five matrices of

luminance pixels, the first five matrices of decoded chrominance pixels, and the second five matrices of decoded chrominance pixels are stored at memory addresses that are offset by a power of two from memory addresses storing each one of the another first five matrices of luminance pixels, the another first five matrices of decoded chrominance pixels, and the another second five matrices of decoded chrominance pixels.